A Two Stage Power Converter Topology for High Voltage DC Power Supplies Under Pulsed Loads

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Summary

High voltage power supplies for radar applications are investigated, which are subjected to high frequency pulsed load (above 100 kHz) with stringent specifications (regulation < 0.01%, efficiency >85%, droop < 0.5 V/micro-sec.). As good regulation and stable operation requires the converter to be switched at much higher frequency than the pulse load frequency, transformer poses serious problems of insulation failure and higher losses. The solution to this problem as a single stage converter is very difficult. In converters operating at high voltage and high frequency, the insulation failure of high voltage transformer is very common. Skin and proximity effect result in higher power losses. Because of high turns ratio, the winding capacitance results in delays and current spikes. Hence a two-stage converter has been proposed. It isolates the HV transformer from high frequency requirement of the regulation. Its block diagram is shown in the following figure. One stage of it, namely, Base power supply (BPS), operates at low frequency and produces majority of the output voltage and power. The other one, namely, fast power supply (FPS), operating at high frequency and low output voltage supplies the remaining power and takes care of the transient variations of line and load and provides the required regulation. The final output voltage is obtained as sum of the outputs of BPS & FPS. Each of the BPS & FPS use phase modulated-series resonant converter as the power-processing unit with zero voltage switching (ZVS). This topology also allows load frequency variation over a certain range.

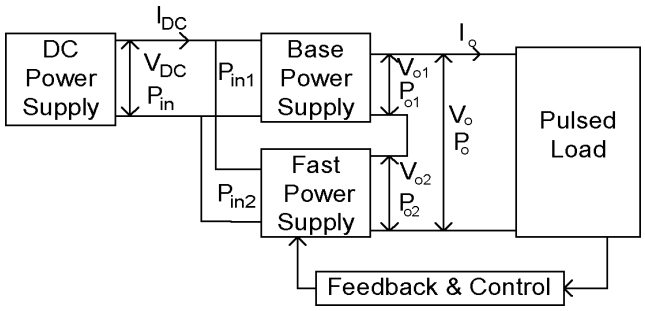


Fig. 0: A two stage Power Conversion

Introduction

High voltage (HV) power supplies are used in industrial, medical, and air-borne applications [1]-[3]. In many such applications, high quality power is required. Radar power supplies are subjected to pulsed load. Pulse load frequency is termed as pulse repetition frequency (PRF). Design of such power supplies is very critical from the aspects of selection of converter topology, switching frequency, control technique, etc.

HV transformer is a critical element in HV power converters due to large number of secondary turns and insulation requirements, which exacerbate its non-idealities like winding capacitance and leakage reactance. Attempts have been made to absorb these non-idealities as useful elements. It has resulted in use of series, parallel, and series-parallel resonant converters (i.e., SRC, PRC, & SPRC respectively). Constant frequency phase modulation is a preferred control technique [4, 5], which yields optimum design of reactive elements. Figs. 1, 2, and 3 show phase-modulated resonant converter, equivalent circuit of HV transformer and various resonant tank circuits respectively. The SRC is free from possible saturation of HV transformer, allows capacitive filter at the output, absorbs transformer leakage inductance (L_1), and gives high efficiency over wide load variations. Its only drawback is not utilizing the transformer winding capacitance. The PRC absorbs the winding capacitance into its tank circuit. But it requires an LC filter at the output. [6] shows that capacitive filter can be used with PRC without degrading the performance. Even then PRC has limitations like, transformer saturation, and low efficiency at light loads. SPRC absorbs both parasitic elements of the HV transformer into its resonant tank. Its efficiency is better than PRC but not as high as SRC. Though in [7], it has been proposed for high voltage pulsed load application, a complicated control strategy is adopted for minimizing conduction and switching losses. SPRC is complex to analyze and difficult to control. Hence, SRC is considered as best converter topology for high voltage and high power applications.

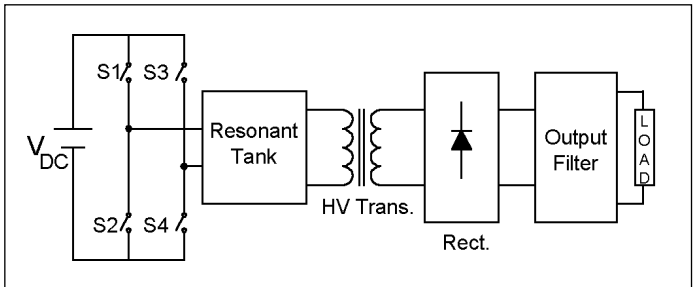


Fig. 1: Phase modulated resonant converter

A limited literature is available in the area of high voltage pulsed load applications. Using SRC, few control methods are proposed for pulsed load applications. In [8], SRC is controlled by an offset voltage comparator for voltage regulation, which inhibits further resonant pulses if the output voltage is within certain error band. Theoretical accuracy of such a converter is determined by the voltage rise of the output capacitor with the energy in one resonant current pulse. A regulation of ± 0.25 % and an efficiency > 92 % is achieved. In [9], a resonant inverter is controlled by a comparator control technique. Between two consecutive load pulses, during on time, the on-off control charges the output capacitor by certain integral number of current pulses to the required potential. For few kHz of PRF, < 0.005 % regulation is achieved with an efficiency of 95 %. In case of PRFs of few tens of kHz, the inverter switching frequency needs to be raised considerably to achieve the same regulation. Hence, for higher PRFs, these methods give satisfactory efficiency but not regulation.

Presently, performance requirements are met by suitable control strategy and insulation requirements are met by low switching frequency of the converter. This paper proposes a two-stage converter topology, which can handle high as well as variable PRFs providing tight output voltage regulation and high efficiency. The two-stage converter's performance is compared with a single-stage converter of same ratings and switching frequency. It is observed that regulation obtained by single-stage converter is much inferior than proposed converter and efficiency of single-stage converter is just 1 % higher than that of the proposed converter.

In the proposed converter, PRFs above 100 kHz are considered. Table-1 and Fig. 4 describe the specifications used for the prototype. Actual application may have few tens of kV and few kW as output voltage and power respectively.

Issues of concern with high PRF loads

HV power supplies under pulsed load add more complexities to the converter design as compared to the static load. Good regulation requires switching frequencies one order of magnitude higher than the PRF.

The problems associated with high voltage and high frequency converter are as follows:

– insulation failure of HV transformer;
– increased iron losses and copper losses;
– due to large turns ratio of HV transformer, increased leakage inductance increases switching/snubber losses and results in poor regulation; large winding capacitance results in current spikes, delay and distortion in the converter waveforms;
– at high frequencies, parasitic elements of the converter may become comparable to actual circuit elements.

Hence, proper converter topology and control techniques are required to meet the application needs. In the proposed two-stage converter, phase-modulated series resonant converter is used as the basic power-processing unit. Next section briefly describes its operation, design in general and also with reference to HV power supplies.

Table 1:	
DC Supply Voltage: 270 V ± 10 %	Regulation: < 0.01 %
Output Voltage: 1 kV	Droop: 0.5 V/μ sec.
Peak Power: 6 kW	PRF: 100 to 125 kHz
Average Power: 600 W	Efficiency: > 85 %

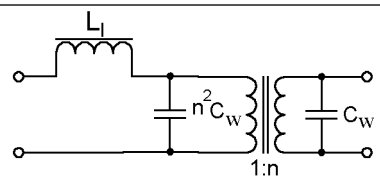


Fig. 2: HV transformer equivalent ckt

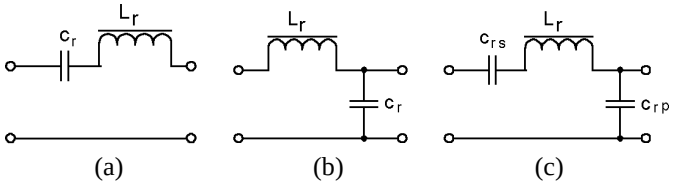


Fig. 3: Resonant tank circuits (a) series resonant ckt, (b) parallel resonant ckt., (c) series-parallel resonant ckt.

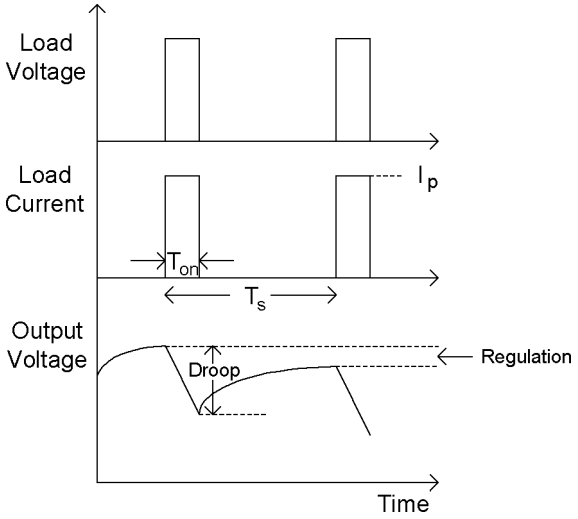


Fig. 4: Load waveforms describing specifications

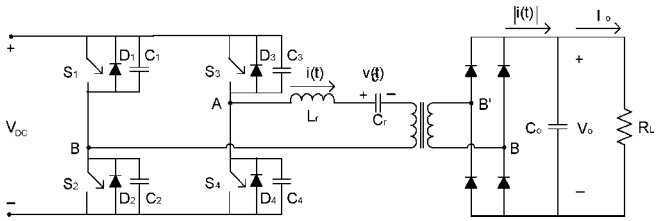
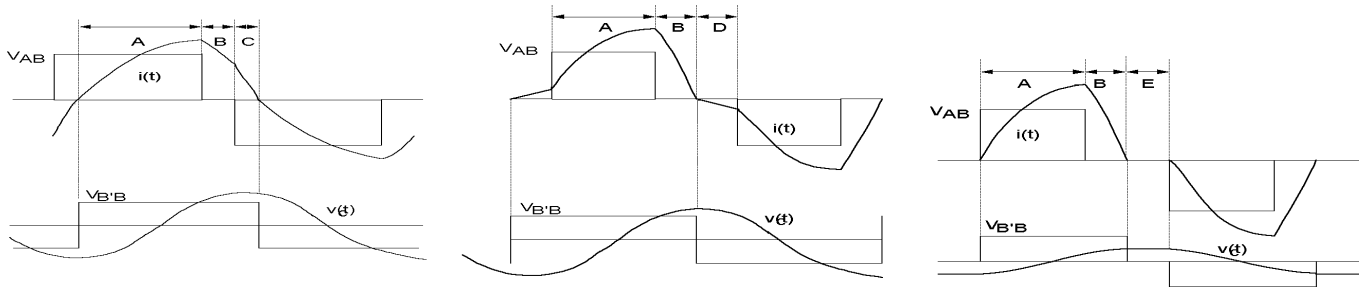


Fig. 5: Phase-modulated series resonant converter

Phase-modulated series resonant converter

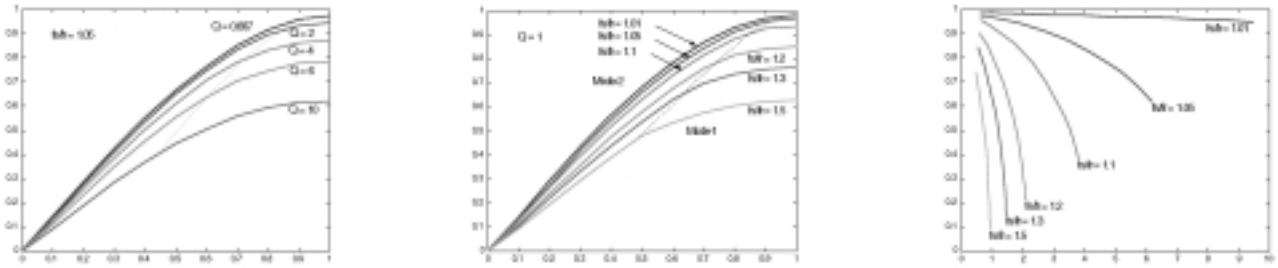
Phase-modulated series resonant converter (PM-SRC) shown in Fig. 5 is most suitable for high-voltage DC power supplies. Switching the converter at a frequency higher than the resonant frequency, facilitates zero voltage switching (ZVS) of the devices with the aid of capacitors connected across them. It operates in three modes, namely, mode-1, mode-2, and mode-3. Fig. 6 shows tank current, $i(t)$, inverter output voltage, V_{AB}, resonant capacitor voltage, $v_c(t)$, and $V_{B'B}$, under the three modes. *A, B, C, D,* and *E* are the various sub-periods.

Design of this converter involves selection of suitable operating point, design of resonant tank elements, output filter, and feedback loop [10]. These are described as follows.



(a) Mode-1 operation (b) Mode-2 operation (c) Mode-3 operation

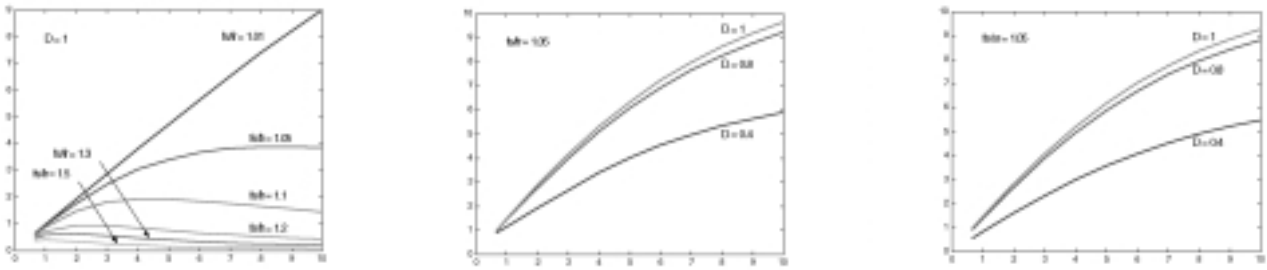
Fig. 6: Modes of operation



a) Voltage gain vs. duty cycle (varying Q)

(b) Voltage gain vs. duty cycle (varying f_s/f_r)

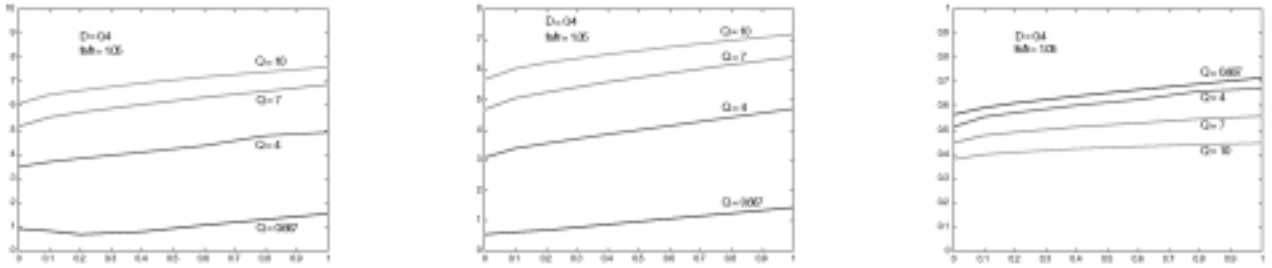
(c) Voltage gain vs. load current (varying f_s/f_r)



(d) Output power vs · Q (varying f_s/f_r)

(e) Peak tank current vs · Q (varying D)

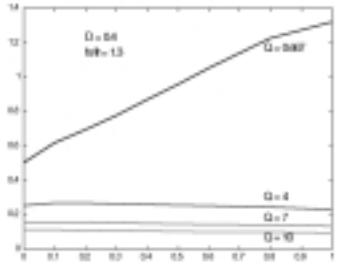
(f) Peak capacitor voltage vs · Q (varying D)



(g) Peak tank current vs · C_w, (varying Q)

(h) Peak capacitor voltage vs · C_w, (varying Q)

(i) Voltage gain vs · C_w, (varying Q, f_s/f_r = 1.05)



(j) Voltage gain vs · C_w, (varying Q, f_s/f_r = 1.3)

Fig. 7: Design graphs

Selection of operating point

Operating point is a function of switching frequency (f_s), ratio of switching frequency to resonant frequency (f_s/f_r), and quality factor (Q). Selection of f_s depends on efficiency, power density, input voltage, and power to be handled. In HV applications, usually a moderate f_s is selected (50-100 kHz). $f_s/f_r > 1$ for ZVS operation. A range of 1.05 to 1.2 is used. A specific value depends on converter gain, margin for ZVS operation, transient response, and minimizing the effect of winding capacitance of HV transformer (C_w). Once f_s and f_s/f_r are determined, f_r can be calculated. Selection of Q depends on the gain, ZVS range, peak tank stresses, and minimizing the effect of C_w. Usually $C_{w'}(= n^2 \cdot C_w/C_r)$ is useful for design, n is transformer turns ratio. Lower Q results in higher gain, lower tank stresses, and larger C_r. Larger C_r helps in minimizing the effect of C_w on converter performance. Higher Q results in lower gain, larger tank stresses and lower C_r. For a $Q = 0.667$, the tank stresses are less than but close to 1 p.u. Graphs of Fig. 7 help in selection of operating point of SRC in general as well as for HV applications. These are obtained analytically with computer simulation under ideal conditions.

Design of resonant tank elements

Design of resonant tank elements requires selection of converter gain (M) and Q of the converter. All the relevant parameters are grouped in the following expressions.

$$n = \frac{V_0}{M \cdot V_{DC}}$$

$$Q = \frac{Z_c}{R_{L'}} \text{ where, } R_{L'} = \frac{R_L}{n^2}, \text{ and } Z_c = \sqrt{\frac{L_r}{C_r}}$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$$

For HV applications, usually high gain is preferable so that turns ratio is reduced. A value $M \geq 0.9$ is advisable. For high gain, low value of Q is selected. For fixed load, a low Q is advisable and for variable load, relatively higher Q is preferred. A range of 0.667 to 4 may be used. Then from the above expressions L_r and C_r are computed.

Output filter

For pulsed load applications, filter capacitor selection depends on the allowable droop. It is selected with the help of following expressions. These are with reference to Fig. 4.

charge supplied during pulse load = $\Delta Q = I_p \times T_{on}$

change in the output voltage during pulse load = ΔV_0 = droop $\times T_{on}$

filter capacitor = I_p/droop

Feedback loop

Fig. 8 shows the output voltage response of a PM-SRC for a step change in control signal. It can be approximated as first order response. Hence control to output transfer function may be expressed as

$$G(s) = \frac{\hat{v}_o}{\hat{d}} = \left(\frac{G}{1+s\tau}\right)$$

where, $\hat{V}_o$ = perturbation in the output voltage, $\hat{d}$ = perturbation in the duty cycle, G = control to output gain, and τ = time constant

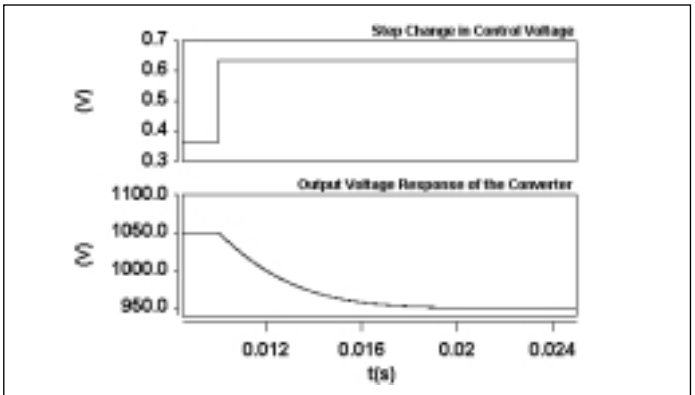


Fig. 8: Step response of PM-SRC

of open loop system. Hence a simple PI-controller is sufficient to regulate the output voltage.

Beat frequency oscillations under pulsed loading

In HV power supplies, it is preferable to have capacitive output filter than LC filter due size constraints. SRC requires only capacitive filter as the resonant tank converts the inverter output voltage into current, which after rectification can be filtered directly by a capacitor. Figs. 9(a) and (b) show two capacitor charging systems, one with constant current source and the other with pulsed current source respectively. In both the situations load is pulsed in nature. With constant current source, the output voltage waveform is steady and has zero regulation. It is true for all PRFs as equal amounts of charge are supplied to the output filter between two consecutive load pulses. It is shown in figs. 9(c) and (d) for PRFs of 125 and 500 kHz respectively. In practice, pulsed current source is used. Based on the frequency of source current pulses, relationship between source frequency & PRF, and their relative phase, beat frequency oscillations may appear in the output voltage. Unequal amounts of charge may be supplied to the output capacitor between two consecutive load pulses. It results in inferior regulation. This effect is shown with simulation for a source frequency of 125 kHz and PRFs of 100 and 250 kHz in Figs. 9(e) and (f) respectively. These oscillations are present in Fig. 9(e) but not in Fig. 9(f) with max. regulations of 0.0045 % and 0.0078 % respectively.

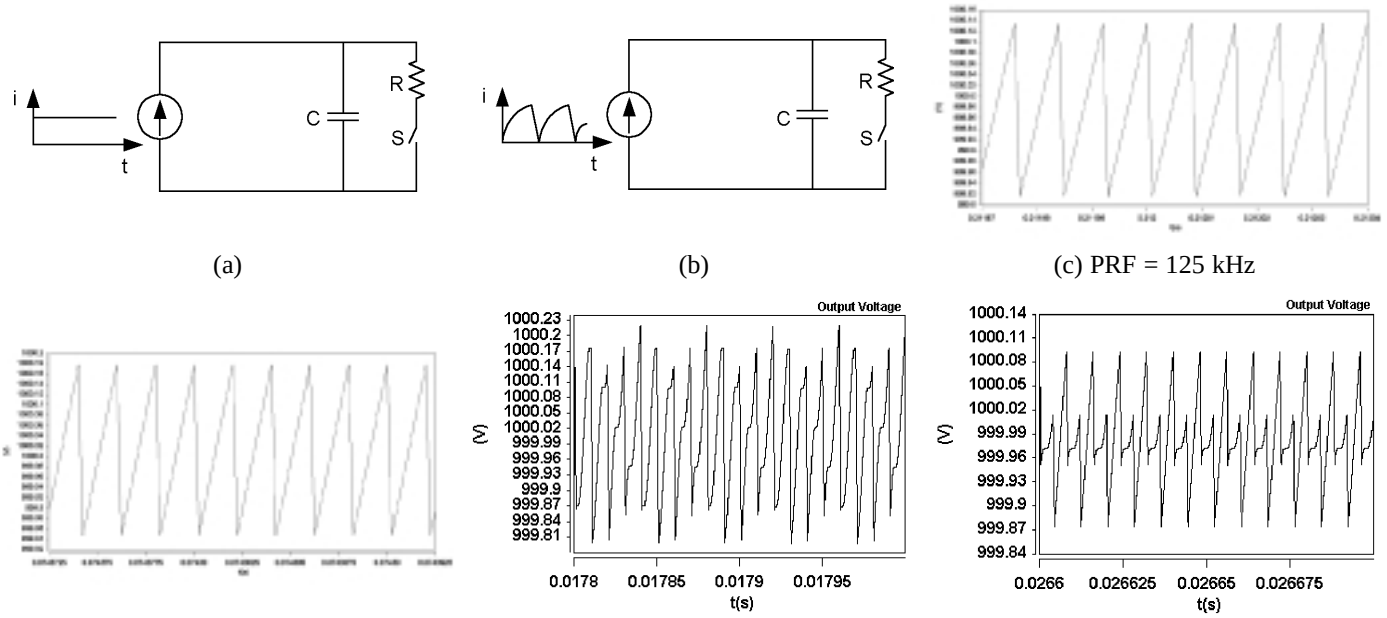
Effect of beat frequency oscillations is of importance under stringent output voltage regulation (< 0.001%). This effect can be eliminated if source and load pulses are synchronized. But synchronization is not practical under variable PRF or very high PRF. Under such situation, this effect can be minimized by the proposed converter topology as shown in further in this paper.

Proposed power converter topology

A power converter topology named as output voltage modulated (OVM) power converter is proposed for high and variable PRF application. The block diagram is shown in Fig. 10(a) and the circuit diagram in Fig. 10(b). In these figures, the parameters have their usual meaning.

Principle of operation

Two PM-SRCs named as base and fast power supplies (BPS & FPS) are operated from a common voltage source (V_{DC}). Their output voltages (V_{o1} & V_{o2}) are summed to produce the load voltage (V_o). Voltage regulation is achieved through duty cycle control of FPS as BPS is uncontrolled and operates in mode-1. BPS produces majority of the output voltage and power, whereas,



(a) (b) (c) PRF = 125 kHz

(d) PRF = 500 kHz (e) PRF = 100 kHz (f) PRF = 250 kHz

Fig. 9: Beat frequency oscillations

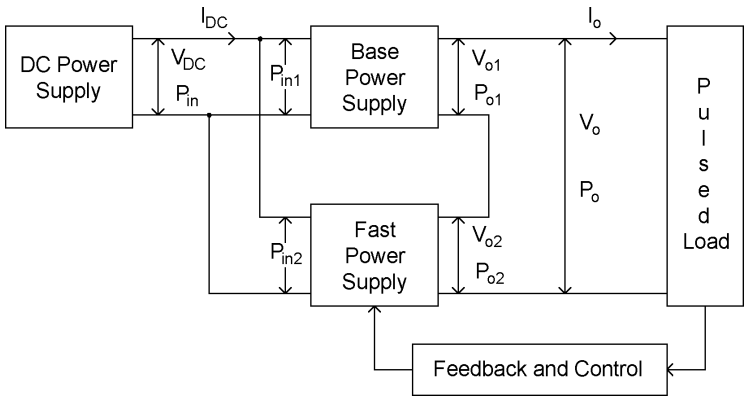


Fig. 10(a): Block diagram of OVM converter

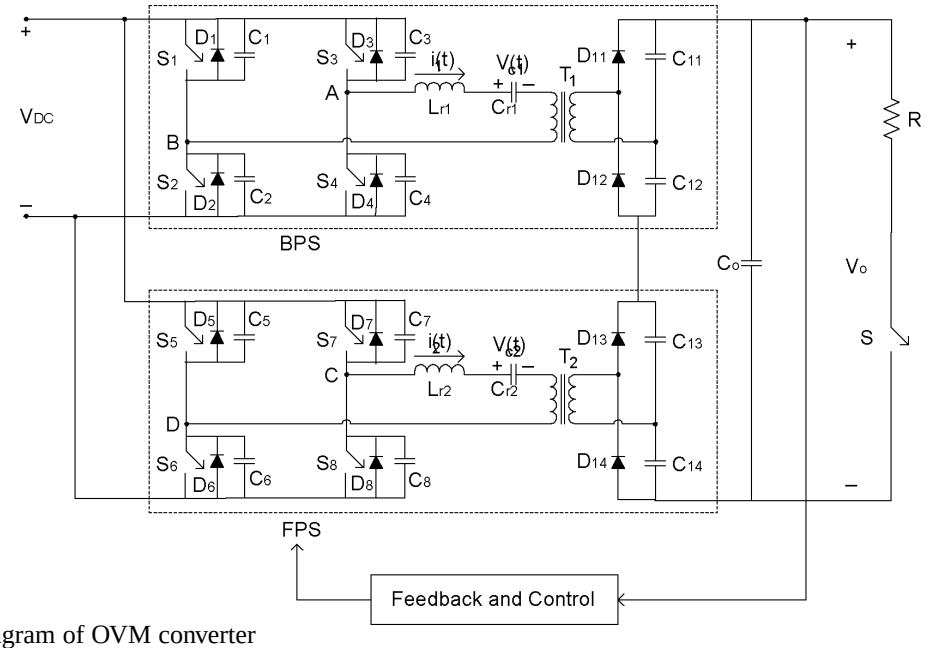


Fig. 10(b): Circuit diagram of OVM converter

the balance is produced by FPS. In actual application, output of BPS can be few kV. A moderate switching frequency (< 100 kHz) can alleviate the problems of HV transformer. Output of FPS is only few hundreds of volts to few kV. It can be switched at much higher frequency for good regulation. ZVS is always ensured for BPS providing efficiency > 90 %. Additional means is required for ZVS of FPS as it undergoes mode-2 operation with efficiencies close to 80 %. Overall efficiency of the OVM converter depends on BPS and is high. Control to output characteristic of OVM converter is of first order. A PI-controller is sufficient for the closed loop operation.

Voltage and power division between BPS and FPS

BPS is designed for rated load at maximum input voltage. FPS is designed at minimum input voltage to produce the balance of output voltage and power. Power handled by BPS and FPS are dependent on their output voltages as their output currents are same. Assuming the converter components to be ideal and neglecting the droop,

$V_o = V_{o1} + V_{o2}$

under maximum input voltage, $V_{o2} = 0$

and, $V_o = V_{o1} = (1 + X) \cdot G \cdot V_{DC}$ (1)

under minimum input voltage,

$V_{o1} = = (1 - X) \cdot G \cdot V_{DC}$

$V_{o2} = V_{o2(max)} = [V_o - G \cdot (1 - X) \cdot V_{DC}]$ (2)

where, X = % variation of the input voltage, V_{DC} = nominal input voltage of BPS and FPS, and G = gain of BPS. Using equations (1) and (2),

$V_{o2(max)} = [(1 + X) \cdot G \cdot V_{DC} - (1 - X) \cdot G \cdot V_{DC}] = 2X \cdot G \cdot V_{DC}$

and

$$\frac{V_{o2(max)}}{V_o} = \frac{2X}{(1+X)}$$

hence,
max. % of the voltage to be produced by FPS = $2X/(1 + X) \times 100$
max. % of the power to be handled by FPS = $2X/(1 + X) \times 100$.

Overall efficiency of the OVM converter

Let, η_1 = efficiency of the BPS, η_2 = efficiency of the FPS, from Fig. 10(a),

$P_{in} = P_{in1} + P_{in2} = V_{DC} \cdot I_{DC}$ (3)

$P_o = P_{o1} + P_{o2}$ (4)

$$\text{Let, } K = \frac{P_{o2}}{P_{o1}} = \frac{V_{o2} \cdot I_o}{V_{o1} \cdot I_o} = \frac{V_{o2}}{V_{o1}}$$

Using equations (3) and (4),

$$\frac{1}{\eta} = \frac{P_{in1}/P_{o1}}{1+P_{o2}/P_{o1}} + \frac{P_{in2}/P_{o2}}{1+P_{o1}/P_{o2}} = \frac{1/\eta_1}{1+K} + \frac{1/\eta_2}{1+1/k}$$

$$= \frac{1}{(1+K)} \cdot \left(\frac{1}{\eta_1} + \frac{K}{\eta_2}\right)$$

Hence,

$$\eta = \frac{\eta_1 \cdot \eta_2 (1+K)}{(\eta_2 + K\eta_1)}$$

or

$$\eta = \eta_1 \cdot (1+K) / \left(1 + \frac{K\eta_1}{\eta_2}\right).$$

Efficiency expression is a function of K, η_1, and η_2. K is always less than unity and $(\eta_1/\eta_2) > 1$ for all input conditions.

for K = 0, $\eta = \eta_1$ and

for K > 0, $\eta < \eta_1$.

At the same time, η is close to η_1. Hence η is mainly dependent on η_1.

Transformer turns ratios of BPS and FPS

Let n_1 and n_2 be the transformer turns ratios of BPS and FPS whereas n be transformer turns ratio of an equivalent single stage power converter. All these turns ratios are calculated for same value of gain of individual converters.

Then $V_o = n \cdot G \cdot V_{DC(min)}$

$V_{o1} = n_1 \cdot G \cdot V_{DC(min)}$

$V_{o2} = n_2 \cdot G \cdot V_{DC(min)}$

Also $V_o = V_{o1} + V_{o2}$

Hence, $n = n_1 + n_2$

As $n_1 < n$, splitting the power conversion in two stages reduces the turns ratio of the HV transformer as well as magnitude of reflected winding capacitance.

Selection of switching frequencies for BPS and FPS

For satisfactory performance of the OVM converter, switching frequency of BPS (f_B) can be moderate and that of FPS (f_F) should be high. In PM-SRC, frequency of the rectified tank current is twice the converter switching frequency. Hence, f_B and f_F are selected such that

$2 f_B = N_1 \cdot PRF_{(max)}$

$2 f_F = N_2 \cdot PRF_{(max)}$

where, N_1 and N_2 are integers.

There can be a situation that maximum PRF is large enough such that half of its value itself is not acceptable as switching frequency of BPS. Under this condition, f_B should be selected as 1/4 of the maximum PRF. With this, frequency of the rectified tank current of BPS becomes half of the maximum PRF. As BPS always operates in mode-1, the tank current waveform is close to sine wave. Hence, the charge supplied by the BPS to the output filter capacitor between any two consecutive load pulses will not differ considerably. It results in best possible regulation even under very high PRFs (up to 400 kHz).

In this paper, maximum PRF is taken as 125 kHz with 20% variation below it. Hence, f_B and f_F are selected as 62.5 and 250 kHz respectively.

Control technique

Splitting the power supply as BPS and FPS helps in tackling the low frequency and high frequency needs of the power conversion. Due to BPS, FPS, and pulsed load, three different frequencies are introduced in the output stage. It may result in beat frequency oscillations and inferior regulation of output voltage, which is more pronounced for variable PRF.

In Fig. 10(b), output filter is a parallel combination of C_0 and series connection of C_{11} to C_{14}. Let, $C_{11} = C_{12} = C_B$ and $C_{13} = C_{14} = C_F$. Secondary currents of BPS and FPS transformer charge the output filter. Secondary current of BPS transformer divides into two parts. During the positive half cycle, a part of the current is through C_{11} and the remaining is through C_0, C_{14}, C_{13} and C_{12}. Similarly negative half cycle divides into two parts. Again, similar process occurs for the secondary current of the FPS transformer.

As mentioned earlier, C_0 is selected much larger than C_B or C_F. For good regulation, replenishing of charge on C_0 between any two consecutive load pulses should be made dependent on FPS and almost independent of BPS. Large value of $2f_F$ reduces the charge associated with each current pulse. Even under non-integral multiplicity of $2f_F$ with PRF, very good regulation can be achieved (< 0.005 %). It is possible by having high value of C_B:C_F. Thus most of the charging current from BPS is utilized by C_B itself. For FPS, equivalent capacitances of the two parallel paths are still comparable. Hence, charging of C_0 is mainly done by the FPS. This effect is shown in Figs. 11(a) and (b) for a PRF of 100 kHz with C_B:C_F of 1:1 and 15:1 respectively. This can be noticed by comparing the waveforms of charging current of C_0 with that of C_{13}. For C_B:C_F of 15:1, they become steady and almost equal. For output voltage of 1 kV, Table 2 shows the effect of C_B:C_F on regulation under variable PRF. In this table, regulation is expressed in mV for ease in comparison.

From the above table, following inferences can be drawn:

– splitting of the power converter as BPS and FPS improves the regulation;
– increasing C_B:C_F improves regulation; this is significant when $2f_F$ is integral multiple of PRF;
– for PRFs close to frequencies which form integral multiplicity with both BPS and FPS, the regulation is very good; there is no significant effect with variation of C_B:C_F.

For C_B:C_F of 15:1 and a PRF of 250 kHz, a regulation of 1.5 mV is achieved.

Results

The proposed converter is built for the specifications mentioned earlier and its performance is studied through simulation as well as experiment. The converter is designed for a quality factor of 0.6667 and $f_s/f_r = 1.05$. Based on the design procedure explained, values of the components for BPS and FPS are as follows.

For BPS: $L_{r1} = 260.08\ \mu H$, $C_{r1} = 27.5$ nF, $n_1 = 1.69$

For FPS: $L_{r2} = 233.88\ \mu H$, $C_{r2} = 1.91$ nF, $n_2 = 0.38$

Table 2: Effect of C_B:C_F on regulation

PRFs (kHz)	Regulation (mV) for C_B:C_F: of 1:1	5:1	10:1	15:1
100	22	7	4	2
105	27	19.5	15	12.5
110	26	24	22	22
115	19	19	19	18.5
120	11	11	11	10.5
125	≈ 0	≈ 0	≈ 0	≈ 0

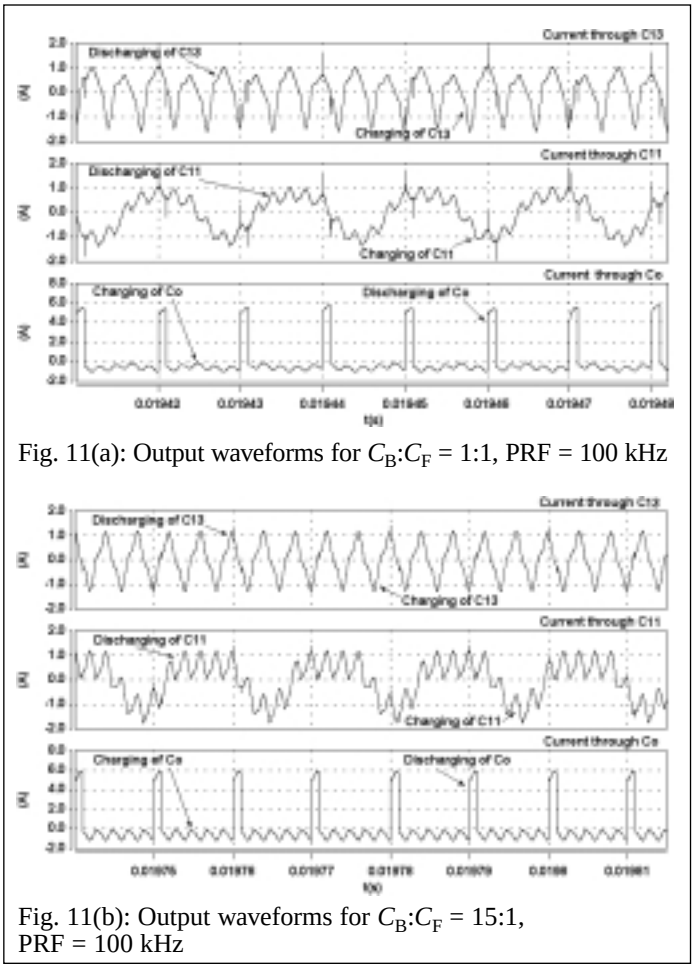


Fig. 11(a): Output waveforms for C_B:C_F = 1:1, PRF = 100 kHz

Fig. 11(b): Output waveforms for C_B:C_F = 15:1, PRF = 100 kHz

Inverter waveforms of BPS & FPS

Inverter waveforms of BPS & FPS are for nominal input voltage. Figs. 12(a) to (d) are for BPS. Fig. 12(a) shows inverter output voltage and tank current, Fig. 12(b) shows resonant capacitor voltage, and Figs. 12(c) and (d) show turn-on and turn-off transients respectively for left-leg of the inverter showing ZVS operation. Figs. 13(a) to (d) are for FPS. Fig. 13(a) shows inverter output voltage and tank current, Fig. 13(b) shows resonant capacitor voltage, and Figs. 13(c) and (d) show turn-on and turn-off transients respectively for left-leg of the inverter showing ZVS operation.

Transient behavior of OVM converter

Figs. 14(a) and (b) show the step response under simulation and experiment. For a step change in control signal of FPS, responses of V_{o1}, V_{o2}, and V_o are observed. A change in V_{o2}, results in change in the loadings of both converters. Due to slow response of BPS, V_{o2} also settles slowly. Hence, overall step response is determined mainly by BPS giving first order control to output characteristic. A PI-controller suffices for the closed loop operation.

Load voltage waveforms & beat frequency oscillations

Fig. 15(a) shows the simulation waveforms of load current, load voltage, and total output voltage for a PRF of 125 kHz. Fig. 15(b)

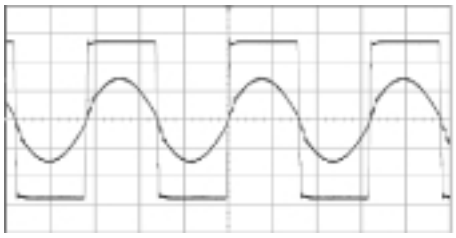


Fig. 12(a): BPS inverter output voltage and tank current
(Voltage: 100 V/div., Current: 2 A/div., Time: 5 µsecs./div.)

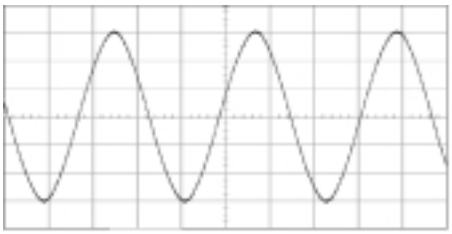


Fig. 12(b): BPS resonant capacitor voltage
(Voltage: 100 V/div., Time: 5 µsecs./div.)

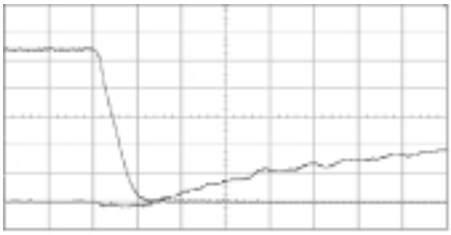


Fig. 12(c): BPS left-leg ZVS turn-on transient
(Voltage: 50 V/div., Current: 1 A/div., Time: 200 nsecs./div.)

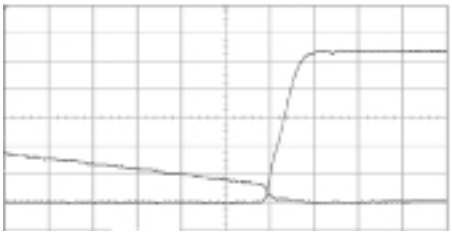


Fig. 12(d): BPS left-leg ZVS turn-off transient
(Voltage: 50 V/div., Current: 1 A/div., Time: 200 nsecs./div.)

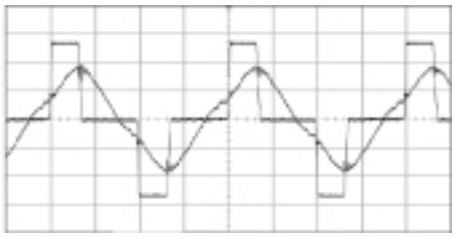


Fig. 13(a): FPS inverter output voltage and tank current
(Voltage: 100 V/div., Current: 0.5 A/div., Time: 1 µsec./div.)

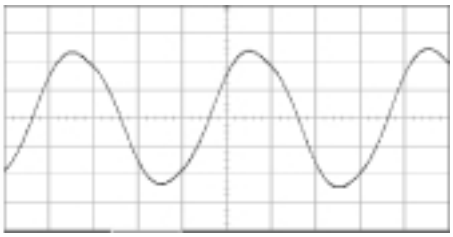


Fig. 13(b): FPS resonant capacitor voltage
(Voltage: 100 V/div., Time: 1 µsec./div.)

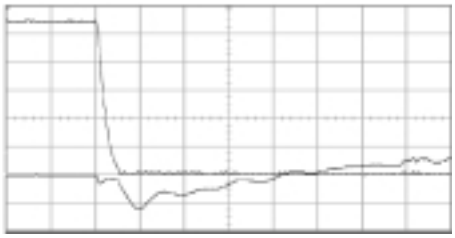


Fig. 13(c): FPS left-leg ZVS turn-on transient
Voltage: 50 V/div., Current: 1 A/div., Time: 200 nsecs./div.)

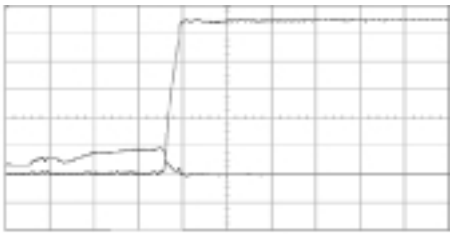


Fig. 13(d): FPS left-leg ZVS turn-off transient
(Voltage: 50 V/div., Current: 1 A/div., Time: 200 nsecs./div.)

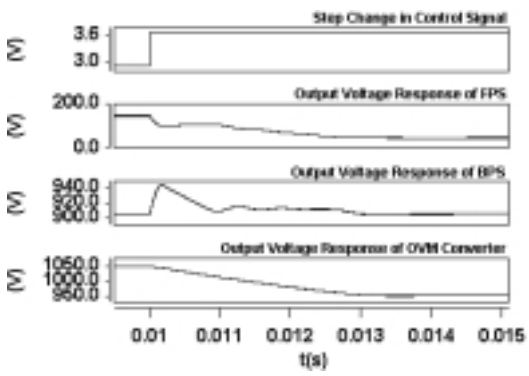
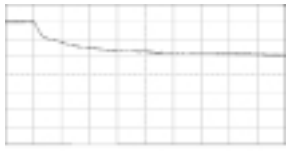
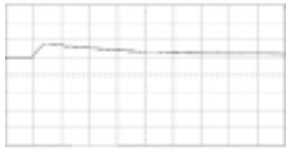


Fig. 14(a): Simulated step-response of OVM converter

Response of FPS
(voltage: 50 V/div., Time: 1msec./div.)



Response of BPS
(voltage: 50 V/div., Time: 1msec./div.)



Response of OVM Converter
(voltage:100 V/div., Time: 1msec./div.)

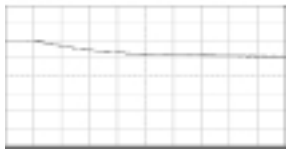


Fig. 14(b): Experimental step-response of OVM converter

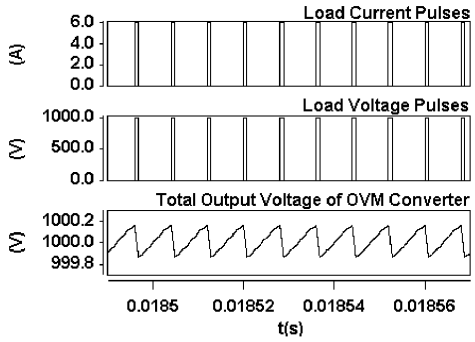


Fig. 15(a): Simulated load waveforms

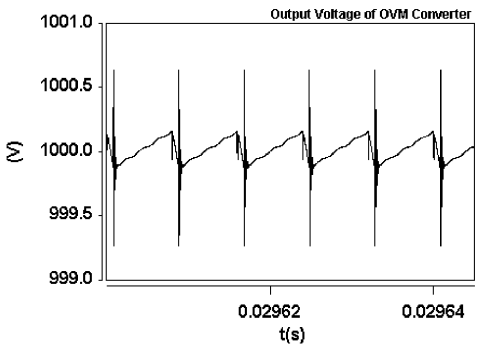


Fig.15(b): Parasitic effect on output voltage

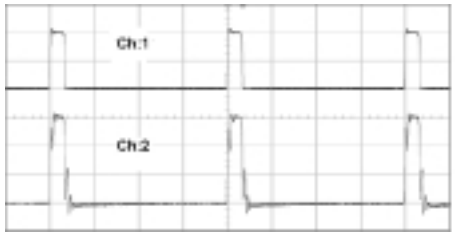


Fig. 15 (c): Experimental load waveforms (Ch:1:Voltage, Ch:2: Current)(Voltage: 500 V/div., Current: 2 A/div., Time: 2 µsecs./div.)

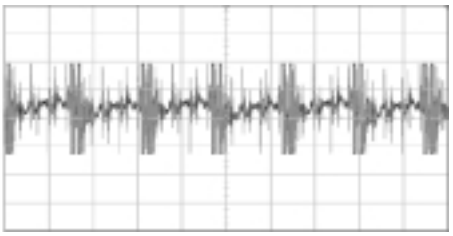


Fig. 15(d): Experimental output voltage waveform (Voltage: 0.5 V/div., Time: 5 µsecs./div.)

Table 3:

For BPS	For FPS
device conduction losses = 10.8 W	device conduction losses = 2.0 W
device turn-off losses = 0.39 W (as turn-off is not true ZVS)	device turn-off losses = 8.1 W (as turn-off is not true ZVS)
transformer & core losses = 5.173 W	transformer & core losses = 1.139 W
transformer & tank copper losses = 2.455 W	transformer & tank copper losses = 0.837 W
output rectifier losses = 2.395 W	output rectifier losses = 3.31 W
Total losses = 21.213 W	Total losses = 15.386 W

shows the effect of parasitic elements on output voltage waveform by simulation. Fig. 15(c) and (d) show the corresponding waveforms experimentally.

Figs. 16(a) to (c) show the output voltage waveforms under simulation for PRFs of 100 115, and 250 kHz respectively. For 250 kHz, switching frequency of BPS is 1/4 of PRF. This shows the performance of this topology under very high PRF operation. Figs. 16(d) to (f) show the output voltage waveforms under experimental condition for the same PRFs respectively. The rise and fall of the load current pulse is about 100 nsecs. The measured droop is 0.4 V/µsec. The regulation achieved under experimental condition closely matches with simulation as given in Table 2. The noise over the waveforms is neglected in the measurement.

Output voltage waveforms under variable PRF operation i.e., Figs. 16(a) and (c) can be compared with Figs. 9(e) and (f) which are equivalent to single stage conversion. Reduction in magnitude of beat frequency oscillation and corresponding improvement in regulation can be clearly noticed with the OVM topology. For PRFs of 100 and 250 kHz, OVM gives a regulation of 0.0002 % and 0.00015 % respectively whereas Single stage converter gives 0.0045 % and 0.0078 % respectively. Hence there is significant improvement with the OVM converter. The noise spikes in these waveforms are due to ESL of the filter capacitors and parasitic inductance of the current paths. Peak load current is high for the prototype as the output voltage is scaled down. Under practical situation this problem should not exist. For the same power and droop, at reduced output voltage more filter capacitance is required. It has resulted in larger area and longer tracks in the output stage further increasing the parasitic inductance.

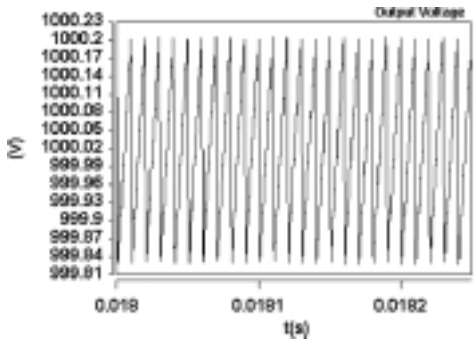
Effect of winding capacitance

Winding capacitance is not absorbed by the SRC. Winding capacitance results in delays and distortions in the converter waveforms. To minimize its effect on converter performance, care needs to be taken while winding the transformer and converter design. Suitable winding technique can minimize the winding capacitance considerably. While selecting the operating point, graphs of Figs. 7(g) to (j) can be used. For low Q, $C_{w'}$ has least effect on tank stresses. For a given Q, when f_s/f_r is closer to unity, $C_{w'}$ has minimum influence on the converter gain. In addition to this, its effect can be noticed in transformer secondary voltage and current. Winding capacitance results in delay in rate of rise of secondary voltage as this capacitance needs to be charged whenever there is a change in the polarity. During this time of charging, a notch can be noticed in the current waveform as the current gets diverted into the capacitance. In the OVM topology, effect of winding capacitance needs to be considered only with BPS as FPS doesn't handle large voltages. Secondary voltage and current waveforms of BPS are shown in Fig. 17.

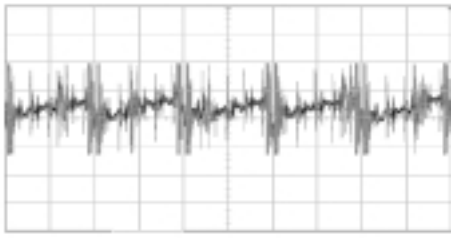
A network analyzer can be used for the measurement of winding capacitance by observing the resonance between the winding capacitance and leakage inductance of the HV transformer. With the values of this resonant frequency and leakage inductance of the transformer, winding capacitance can be calculated. The estimated $C_{w'}$ for BPS transformer is 0.1 nF.

Efficiency of the OVM converter

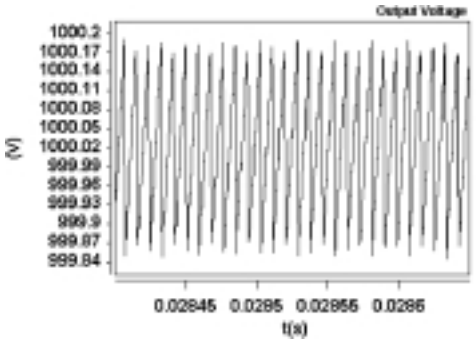
Various losses in the converter are detailed in Table 3 for nominal input voltage.



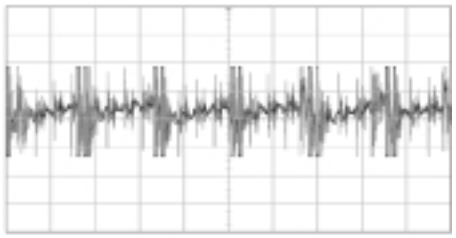
(a) PRF = 100 kHz



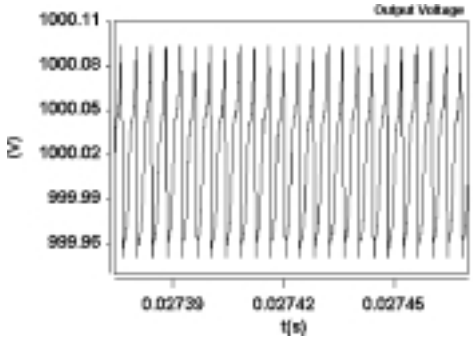
(d) Voltage: 0.5 V/div., Time: 5 μsecs./div., PRF = 100 kHz



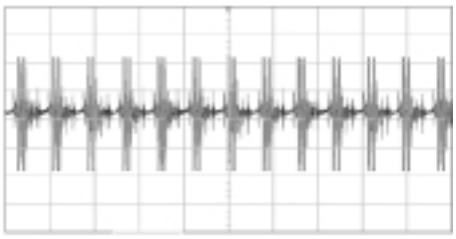
(b) PRF = 115 kHz



(e) Voltage: 0.5 V/div., Time: 5 μsecs./div., PRF = 115 kHz



(c) PRF = 250 kHz



(f) Voltage: 1 V/div., Time: 5 μsecs./div., PRF = 250 kHz

Fig. 16: Output voltage waveforms under simulation (a,b,c) and experiment (d,e,f)

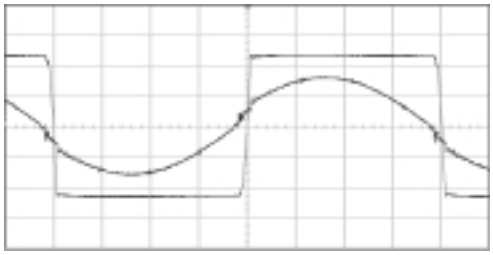


Fig. 17: Waveform showing effect of winding capacitance (Voltage: 200 V/div., Current: 1 A/div., Time: 2 msecs./div.)

Table 4:

V_{DC} (V)	η_1 (%)	η_2 (%)	η (%)
243	95.02	84.45	92.33
270	95.47	78.22	93.5
297	95.76	4.92	92.03

Overall efficiency (η) depends on η_1, η_2, and the ratio K. Table 4 gives these efficiencies under different input voltages. η_2 remains almost constant and is > 95 %. η_2 varies over a wide range as its output power is variable. It has maximum efficiency at lowest input voltage. Overall efficiency is > 92 % in the entire range.

Conclusions

The OVM converter is proposed for high and variable PRF operation. The two-stage power conversion helps in isolating the HV transformer from high frequency switching. Required regulation is achieved through the FPS. Regulation is mainly dependent on the switching frequency of FPS and relative grading of output filter capacitors of BPS and FPS. In the entire range of PRF variation, regulation of the order of < 0.0022 % is achieved. Majority of the output voltage and power are produced by BPS. Voltage and power handled by FPS are only a small percentage (18.18 %) of the total power and depend on the percentage variation of supply voltage. This allows high frequency switching of FPS. Overall efficiency is dependent on BPS efficiency. At nominal input voltage, an overall efficiency > 93 % is achieved for the OVM converter. Under closed loop operation, Q of both BPS and FPS vary. For BPS, Q decreases with increase in supply voltage. For FPS, Q increases with increase in supply voltage. Transient behavior of the OVM converter is mainly dependent on BPS. Control to out-

put characteristic of the OVM converter is of first order requiring only a PI-controller for the closed loop operation.

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